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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,699	03/19/2004	Tim J. Bales	DB001094-000	9148

57694 7590 09/07/2006

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,699	BALES, TIM J.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-9,11,13-15,17-45,64 and 65* is/are pending in the application.

4a) Of the above claim(s) *9,11,13-15,17-19,21-25,27-31,35,36 and 39-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7,8,20,26,32-34,37,38,64 and 65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Claims 64 and 65, previously withdrawn as a result of a restriction requirement, are hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Claim Objections

Claims 25 and 65 are objected to because of the following informalities: Claim 25, line 2, the word, "fabiracted" appears to be "fabricated". Claim 65, line 18, the word, "increased" appears to be "decreased" and on line 19, the word, "decreases" appears to be "increases". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 5, 7, 8, 20, 26, 32-34, 37, 38, 64, and 65 are rejected under 35 U.S.C. 102(b) as being anticipated by Biber et al. (US 5,134,311, hereinafter, "Biber").

Regarding claim 1, Biber discloses a method of correcting impedance curvature in a MOS driver circuit (circuit in Fig. 3), said method comprising:

using a first MOS transistor (48, 52, 56) and second MOS transistor (46, 50, 54) as part of said MOS driver circuit; and

operating said first MOS transistor and said second MOS transistor so as to compensate for changes in output impedance of said first MOS transistor through corresponding changes in output impedance of said second MOS transistor (see abstract; col. 4, lines 49+; see Fig. 4).

Regarding claim 2, Biber discloses using a signal adder circuit (36, since it turns on the transistors in output stage 32 to add more signals to control impedance of the output signal) as part of said MOS driver circuit, wherein said operating comprises:

maintaining a controlled voltage (voltage at its gate) at a first input terminal of said first MOS transistor (gate of 48, 52, 56), and

using said signal adder circuit to provide a differential voltage (bit 1-3, 4-6 in Fig. 8A and 8B) at a second input terminal of said second MOS transistor (gate of 46, 50, 54).

Regarding claim 4, Biber discloses using an amplifier (34 in Figs. 3, 7) to provide an input signal to said signal adder circuit (/COMP in Fig. 8A, 8B).

Regarding claim 5, Biber discloses using said amplifier includes using an output (COMP in Fig. 7) of a differential amplifier (see 34 in Fig. 7) to supply said input signal to said signal adder circuit (/COMP in Fig. 8A, 8B).

Regarding claim 7, Biber discloses a method of correcting impedance curvature in a MOS driver circuit (circuit in Fig. 3), said method comprising:

using a first MOS transistor (48, 52, 56) and second MOS transistor (46, 50, 54) as part of said MOS driver circuit; and

operating said first MOS transistor and said second MOS transistor so as to increase output impedance of said second MOS transistor when output impedance of said first MOS transistor decreases, and to decrease output impedance of said second MOS transistor when

output impedance of said first MOS transistor increases (see abstract; col. 4, lines 49+; see Fig. 4).

Claims 8, 20, 26, 32-34, 37, 38, 64, and 65 are essentially the same in scope as claims 1, 2, 4, 5, and 7, and are rejected similarly.

Regarding claims 64 and 65, as for the limitation, a processor, memory controller, memory device, first bus and second bus, input device, output device, and data storage device, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Response to Arguments

Applicant's arguments filed June 30, 2006 have been fully considered but they are not persuasive.

Regarding claims 1, 7, 20, and 26, applicant argues on page 11 that "Biber is not directed to a method of correcting impedance curvature." However, the recitation, "correcting impedance curvature" is part of a preamble and not recited in the body of a claim. The recitation that "correcting impedance curvature" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

Regarding claims 1, 20, and 37, applicant argues on page 11 that "Biber does not teach or suggest compensating for changes in the impedance of one transistor by implementing corresponding changes in another transistor." However, Biber teaches a first MOS transistor (e.g. 48) and second MOS transistor (e.g. 46) and when transistor 46 is turned off by the control signal from 36, the output impedance of transistor 46 changes to high impedance since it is open circuit. Therefore, the output impedance of transistor 48 is compensated to the impedance of OUTPUT node because transistors 46 and 48 are connected with transistors 42, 50, 52, 54 and 56 in parallel as shown in OUTPUT STAGE 32.

Regarding claims 7, 26, and 32, applicant argues on page 12 that Biber does not teach the recitation, "so as to increase output impedance of said second MOS transistor when output impedance of said first MOS transistor decreases, and to decrease output impedance of said second MOS transistor when output impedance of said first MOS transistor increase." However, Biber teaches, a first MOS transistor (e.g. 48) and second MOS transistor (e.g. 46) and when transistor 46 is turned off by the control signal from 36, the output impedance of transistor 46 increases since it is open circuit when the output impedance of transistor 48 decreases (e.g. 100 ohms to 57.1 ohms) and compensated to the impedance of OUTPUT node (see Table 1 in Fig. 4). Also, Biber teaches that when transistor 46 is turned on by the control signal from 36, the output impedance of transistor 46 decreases since it is closed circuit when the output impedance of transistor 48 increases (e.g. 32.4 ohms to 42.9 ohms) and compensated to the impedance of OUTPUT node (see Table 1 in Fig. 4)

Regarding claims 64 and 65, previously withdrawn as a result of a restriction requirement, are hereby rejoined and fully examined as applicant requested and are rejected as discussed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER